This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-17 (canceled)

Claim 18 (currently amended): A solid-state image sensing apparatus comprising:

an image sensing area in which a plurality of pixels are two-dimensionally arrayed;

a plurality of output channels;

a first driving mode in which pixel signals of pixels in the image sensing area are read out, wherein the read-out pixel signals are output to at least one output channel selected from among the plurality of output channels;

a second driving mode in which pixel signals of odd-numbered columns and pixel signals of even-numbered columns arrayed in the same row in the image sensing area are read-out, wherein the read-out pixel signals are output to a plurality of output channels selected from among the output channels, and wherein the read-out pixel signals of odd-numbered columns and the read-out pixel signals of even-numbered columns are output to different ones of the selected output channels so as to have different phases; [[~~and~~]]

line memories which are arranged between the pixels and the output channels and which temporarily store pixel signals of the pixels selected and read out in the first driving mode or the second driving mode; and

a control circuit which is arranged between the pixels and the line memories and which sets a driving mode to one of the first driving mode and the second

driving mode based on an externally input signal ~~[[, wherein the input signal]]~~ which may be freely set,

wherein the number of output channels to which the pixel signals are output in the first driving mode and the number of output channels to which the pixel signals are output in the second driving mode are different.

Claim 19 (currently amended): The solid-state image sensing apparatus according to claim 18, [[~~further comprising line memories which temporarily store selected and read-out pixel signals of pixels,~~]]

wherein the control circuit [[~~is arranged between the pixels and the line memories and~~]] is a transfer switch in which a common control signal is input in every other column.

Claim 20 (previously presented): The solid-state image sensing apparatus according to claim 18, wherein the phase shift between the pixel signals of the odd-numbered columns and the pixel signals of the even-numbered columns is 180 degrees.

Claim 21 (previously presented): The solid-state image sensing apparatus according to claim 18,

wherein the image sensing area is provided with a color filter in Bayer matrix corresponding to the pixels, and

in the second driving mode, pixel signals of pixels in the same color phase among color phase codings defined by the color filters are output from the same output channels.

Claim 22 (previously presented): The solid-state image sensing apparatus according to claim 18, wherein in the first and second driving modes, there is a channel which can be used in common.

Claim 23 (previously presented): The solid-state image sensing apparatus according to claim 18, wherein in both the first and second driving modes, pixel signals of pixels from m X n pieces in the image sensing area are output wherein m and n are integers.

Claim 24 (new): The solid-state image sensing apparatus according to claim 18, wherein the line memories are capacitive elements arranged in every column.